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Manufacturing Process of Copper Paste Sintering and Embedded Resistor Multilayer Microwave Circuit Boards

Xiangshu Ji[1], Xiaohui Zhou[2], Wenxiang Pu[1], Xi Chai[1], Jia Meng[1], Deyu Wang[1]

[1]Zhejiang Wanzheng Electronic Technology Co., Ltd., Jiaxing, Zhejiang, 314107, China

[2]Hangzhou Dianzi University Information Engineering School, Hangzhou, Zhejiang, 311305, China

ABSTRACT

This paper focuses on the manufacturing method and characteristics of a copper paste sintered embedded resistor 24-layer microwave circuit board. The process utilizes Taconic high-frequency resistor materials and involves a multi-step approach to create blind hole embedded resistors, including 7 laminations, 6 blind hole electroplatings, 3 pulse electroplatings, 6 copper paste plug holes, 1 resin plug hole, and panel grinding, along with 14 copper reduction steps and 7 back drilling steps. The process is complex and involves numerous control factors. To address quality issues arising from layer misalignment, expansion and contraction, resistance value control, and the unique processes of copper paste sintering, experimental plans were developed for improvement. The final product meets IPC inspection standards and has received customer approval, indicating that the manufacturing process for this copper paste sintered embedded resistor circuit board is feasible.

KEYWORDS

Sintering process; Embedded resistor; Blind hole embedding; Pulse electroplating; Back drilling

1 Introduction

In the context of the rapid development of artificial intelligence and 5G communication technologies, microwave antenna PCBs, as key components of the RF front end of base stations, are experiencing exponential growth in demand. According to data from the Ministry of Industry and Information Technology, the total number of 5G base stations in China surpassed 3 million in 2023, driving the high-frequency PCB market size to reach 42 billion yuan, with a compound annual growth rate of 18.7%. Against this backdrop, 24-layer copper paste sintered embedded resistor circuit boards have become the preferred carrier for millimeter-wave frequency band (24.25 – 52.6GHz) antennas due to their high-density interconnection, low-loss transmission, and integration advantages. These products need to overcome the process limitations of traditional multilayer boards and achieve high-frequency signal integrity through innovative technologies such as copper paste sintering, cross-blind hole back drilling, and precise control of embedded resistors. This paper will systematically elaborate on the key technology development path and validate the feasibility of the solution through experimental data.

1.1 Core characteristics of 24-layer copper paste sintered embedded resistor circuit boards

1.1.1 High-density multilayer architecture design

As shown in Figure 1, the circuit board adopts a 24-layer stacked structure (16 signal layers + 4 power layers + 4 ground layers), enhancing the density to 80 – 100 lines/cm^2 through three-dimensional wiring, which is a 40% improvement compared to conventional 16-layer boards. The embedded resistor network is distributed across the 6th, 12th, and 18th layers, utilizing Ag-Pd/CuO resistor paste (resistance range 10Ω/□ – 10kΩ/□), combined with through holes and blind holes to form three-dimensional interconnections. The dielectric layers use Rogers RO4835 high-frequency laminate (dielectric constant Dk=3.3, loss factor Df=0.0035@10GHz), paired with 50 – 75μm thick prepreg (PP), effectively suppressing the skin effect and dielectric polarization loss in the millimeter-wave frequency band.

1.1.2 Breakthroughs in copper paste sintering process

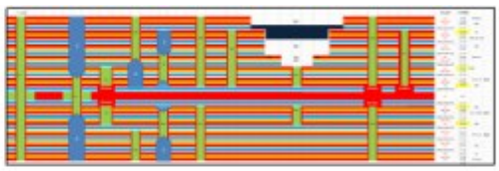
Key processes include:

Resistor formation: Copper-based resistor paste is printed using a 300-mesh stainless steel screen and sintered in a nitrogen environment (peak temperature 850℃ for 30 minutes), forming a 15–20μm thick resistor film with a tolerance of ±5%.

Interface bonding: The peel strength between the copper paste and RO4835 laminate reaches 8.5N/cm (IPC-TM-650 test).

Structural Optimization: Seven back drills are performed to eliminate stubs, with a back drill depth tolerance of ±0.05mm, reducing signal reflection loss (see Figure 2).

(Figure 1)



(Figure 2)

2 Experimental methods and process principles

2.1 R&D experimental methods

2.1.1 Material preparation

High-frequency materials (Taconic TSM-DS3) are cut to the required dimensions.

2.1.2 Inner layer pattern processing (L9-L12)

Etching of L9, L10, and L12 patterns (tolerance ±1mil).
Etching of L11 embedded resistors (tolerance ±1mil).
Gold plating of L9-12 auxiliary images → inner layer gold plating → film removal.
Inspection: Inner layer AOI inspection.

2.1.3 First lamination (L9-L12)

Browning Treatment: Check for color differences and other anomalies before lamination.
Drilling (L9-L12, hole wall roughness ≤25μm).
Copper plating (hole copper ≥25μm).
Resin + copper paste plugging → grinding → copper reduction.
Measure the expansion and contraction of the plugged holes (for subsequent inner layer processing).
Pattern transfer → etching (including L16/L20 embedded resistors) → L7-L8 gold plating → AOI inspection.

2.1.4 Second lamination (L3-L12, L15-L24)

Browning Treatment (same as above).
Drilling (L3-L12/L15-L24) → copper plating.
Back drilling (L3-L12, L19-L24).
Resin plugging → grinding → copper reduction.
Measure the expansion and contraction of the high-frequency laminate.
Pattern transfer → etching → L3-L12 gold plating → AOI inspection.

2.1.5 Third lamination (L1-L24)

Browning Treatment (same as above).
Drilling (L1-L24)→copper plating→back drilling (L1-L12/L15-L24).
Resin plugging→grinding→copper reduction.
Measure expansion and contraction data.
Pattern transfer and etching for L1/L12/L15/L24.
Drilling for L13-L14 (copper plate)→resin drilling→printing and sintering copper paste.
AOI inspection.

2.1.6 Fourth lamination (all layers L1-L24)

Browning Treatment (same as above).
Drilling(through all layers)→copper plating→controlled depth drilling.
Resin plugging→grinding→copper reduction.
Pattern transfer→etching→outer layer AOI inspection.

2.1.7 Post-processing

Solder Mask Production (to prevent solder bridging).
older Mask Curing.
Surface Treatment (tin spraying).
Electrical Performance Testing (open/short circuit testing).
Final Appearance Inspection.

2.2 Production process

Cutting→Inner Layer (blind holes, copper paste) production→four laminations →five copper reductions→four drilling (outer layer through holes)→four plasma treatments→four PTH/CU treatments→three deep drilling→four resin plugging → four copper reductions→re-plating→pattern transfer→inspection→pattern electroplating→etching→inspection→ solder mask→surface treatment→ inspection →first deep milling→second deep milling→third deep milling→shaping→ testing→FQC→packaging.

2.3 Key process control points

Embedded Resistor Precision: By optimizing LDI exposure compensation and developing parameters, the inner layer line width deviation is controlled within ±0.5mil.

Plugging Quality: Resin + copper paste plugging depression ⩽15μm, using aluminum sheet + gas distribution plate plugging technology to enhance fullness to 98.7%.

Sintering Alignment: Screen printing positioning accuracy ±2mil, X-Ray inspection of blind hole alignment.

Thermal Stress Control: After three laminations, board warpage ⩽0.3%, meeting JEDEC MSL-3 level humidity reliability requirements.

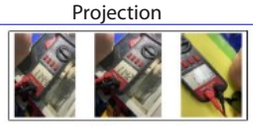
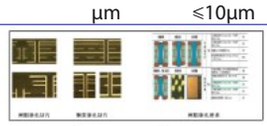
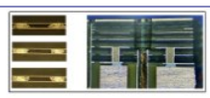
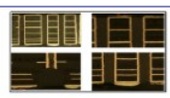
3 Results and discussion

3.1 Electrical performance verification

As shown in Table 1, all tested samples meet technical specifications:

Electroplated Copper Thickness: Average hole copper thickness in blind hole layers is 28.7μm (requirement ⩾25μm),

Table 1

Item		Unit	Technical Requirement	Test Result	Conclusion
Electroplated Copper Thickness (Figure 3)	Finished Coated Copper	μm	>12μm	41.98μm	Pass
	Edge Copper Thickness	μm	⩾20μm	41.9μm	
	Outer Layer Copper Thickness Requirement	Oz/μm	1.50Oz/52.5μm	⩾74.51μm	
Electroplated Copper Thickness (Figure 4)	Blind Hole Layer Copper	μm	⩾25μm	>25μm	Pass
	 (Figure 3)		 (Figure 4)		
Electroplated Gold Thickness	L3/L9 Nickel Thickness	μm	3~5μm	3.12~5.9μm	Pass
	L3/L9 Gold Thickness	μm	0.13~0.45μm	0.136~0.212μm	
	L7 Nickel Thickness	μm	0	0	
	L7 Gold Thickness	μm	⩾2μm	2.0~2.07μm	
Resistance Value (Figure 5)	Inner Layer Resistance Value	Ω	115Ω±5%	114.2~118.6Ω	Pass
Outer Layer Line Width	GTL Surface Line Width	mil	10±1mil	10.52mil	Pass
	GBL Surface Line Width	mil	10±1mil	10.415mil	
Blind Hole Layer Plugging Fullness (Figure 6)	Depression	μm	⩽15μm	10.49μm	Pass
	Projection	μm	⩽10μm	3.64~5.20μm	
	 (Figure 5)		 (Figure 6)		
Copper Paste Sintering (Figure 7)	Dielectric Thickness	mm	>0.09mm	>0.09mm	Pass
	Copper Paste Diameter	mm	>0.3mm	>0.3mm	
	Sintered Copper Paste and Via Alignment	mil	±2mil	±2mil	
Solder Mask Thickness	Solder Mask Film	μm	⩾15μm	18.89μm	Pass
Forming Dimensions	Forming Dimensions	mm	73.95*60.65±0.1mm	73.91*60.59mm	Pass
Blind Slot Dimensions (Figure 9)	Blind Slot Dimensions	mm	±0.075mm		Pass
Reliability (Figure 8)	Thermal Shock		288℃*10 seconds*3	No delamination or voids	Pass
	 (Figure 7)		 (Figure 8)	 (Figure 9)	

outer layer copper thickness is 74.51μm (target ⩾52.5μm).

Resistance Precision: Measured inner layer embedded resistor values range from 114.2–118.6Ω (nominal 115Ω ±5%), with a uniformity CV value ⩽1.8%.

Signal Integrity: Insertion loss in the 28GHz band ⩽0.45dB/inch, return loss ⩽-25dB.

3.2 Structural reliability

Thermal Shock Testing: No delamination or voids after 288℃ for 10 seconds × 3 cycles.

Mechanical Strength: Peel strength 8.2–8.7N/cm (IPC-TM-650 standard ⩾8N/cm).

Dimensional Stability: Forming tolerance ±0.08mm (requirement ±0.1mm), blind slot precision ±0.068mm.

3.3 Process bottleneck analysis

Interlayer Alignment: Cumulative layer offset error after three laminations reached 42μm (limit 50μm), requiring optimization of the thermal riveting positioning system.

High-Frequency Drilling: When deep drilling with a 0.4mm diameter, hole wall roughness fluctuated to 22 – 27μm, suggesting an upgrade to the spindle dynamic balance module.

Copper Paste Brittleness: The bending strength of the sintered resistor film is only 65MPa, necessitating the development of nano-modified pastes to enhance toughness.

4 Conclusion and outlook

The product of this project, "Copper Paste Sintered and Embedded Resistor Multilayer Microwave Circuit Board," achieves cross-blind hole interconnection through seven back drills and copper paste sintering, reducing process complexity by 30%. The integration of embedded resistors reduces the number of peripheral components by 40%, lowering the manufacturing cost per board by 18%, and achieving technological breakthroughs during the research process.

As 6G technology evolves towards the terahertz frequency band, further development of ultra-low-loss dielectrics (Df< 0.001), laser-induced direct writing of copper paste, and other new technologies will be necessary to promote high-frequency PCBs towards 120 layers and above in three-dimensional integration.

About the Author

Xiangshu Ji, Male, Hainan, Graduated from China University of Geosciences, bachelor's degree, Senior Engineer, With 20 years of working experience in PCB product development, technical research, and material research, general manager of Zhejiang Wanzheng Electronic Technology Co., Ltd, Email :jixs0168@163.com.

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